M.R. SIAVASH KATEBZADEH

The University of Edinburgh, Informatics Forum 2.05, EH8 9AB, United Kingdom

Email ◇ Website ◇ Github ◇

WORK EXPERIENCE

CPU Architect Since Jul 2023
Huawei Technologies Research & Development (UK) Ltd *Edinburgh, United Kingdom*

Research Assistant Jan 2023 - Jul 2023
The University of Edinburgh *Edinburgh, United Kingdom*

Postgraduate Researcher 2017 – 2022
The University of Edinburgh *Edinburgh, United Kingdom*
Projects:
– Saba (joint project with Microsoft Research), an application-aware bandwidth allocation scheme designed for RDMA-based datacenter networks and optimized for bandwidth-hungry frameworks (e.g., Apache Spark).
– RPerf (joint project with Microsoft Research), an accurate performance measurement system designed for RDMA-based networks.

Intern 2016
Parallel Systems Architecture Lab, EPFL *Lausanne, Switzerland*
Projects:
– Implementation of CPU timing on QFlex system simulator.
– Detection and elimination of various sources of non-deterministic behavior of QEMU.

Researcher 2014
Software Systems Laboratory, Shiraz University *Shiraz, Iran*
Project: Research on performance optimization of big data workloads on GPU.

Intern 2012
CERT Center (Shiraz APA), Shiraz University *Shiraz, Iran*
Project: Research on pattern-matching algorithms for anti-malware software.

EDUCATION

Ph.D., The University of Edinburgh, Edinburgh, United Kingdom 2017 – 2022
Computer Architecture & Network Communication
Supervisor: Prof. Boris Grot
Thesis title: Performance-Centric Bandwidth Allocation in Datacenters

M.Sc., Shiraz University, Shiraz, Iran 2015 – 2017
Software Engineering
Supervisor: Dr. Farshad Khunjush
Thesis title: Implementation of a Deterministic Functional Simulator
GPA: 18.88/20, 3.83/4, Ranked First

B.Sc., Shiraz University, Shiraz, Iran 2010 – 2014
Software Engineering
Advisor: Dr. Reza Sameni
GPA: 16.83/20, GPA in CS Courses: 18.13/20

RECENT PUBLICATIONS

Saba: Rethinking Datacenter Network Allocation from Application's Perspective 2023
M.R.S Katebzadeh, P. Costa, B. Grot
In European Conference on Computer Systems (EuroSys)

Evaluation of an InfiniBand Switch: Choose Latency or Bandwidth, but Not Both 2020
M.R.S. Katebzadeh, P. Costa, B. Grot
In International Symposium on Performance Analysis of Systems and Software (ISPASS)

Hermes: Fast, Fault-Tolerant and Linearizable Data Replication 2020
A. Katsarakis, V. Gavrielatos, M.R.S. Katebzadeh, A. Joshi, B. Grot, V. Nagarajan, A. Dragojevic
In International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

Bankrupt Covert Channel: Turning Network Predictability into Vulnerability 2020
D. Ustiugov, P. Petrov, M.R.S. Katebzadeh, B. Grot
In USENIX Workshop on Offensive Technologies (WOOT), co-located with USENIX Security

Smart Priority Assignment in Datacenter Networks 2020
M.R.S. Katebzadeh, P. Costa, B. Grot
In the second Young Architect Workshop (YArch)

TECHNICAL SKILLS

Programming	Python, C, C++, Rust, Java, Dart, JavaScript, React, Flutter
System Libs	InfiniBand Verbs, OpenMP, PThreads, MPI, CUDA
Miscellaneous	Proxmox VE, Docker, Git, LaTeX, Shell Scripting

COMMUNITY SERVICES AND PROFESSIONAL ACTIVITIES

- **HPCA'2024**
  – Web co-chair at the 30^{th} International Symposium on High-Performance Computer Architecture
- **MICRO'2022**
  – Submission co-chair at the 55^{th} International Symposium on Microarchitecture
  – Implementation of PiCkeR, a conference management toolkit for program chairs
- **ISCAConf Website**
  Creator and maintainer of the main ISCA conference website and archive at https://iscaconf.org
- **CADS & AISP'2012**
  Technical services assistant at the 16^{th} International Symposium on Computer Architecture & Digital Systems and Artificial Intelligence & Signal Processing

LANGUAGES

- **Farsi/Persian**, Native
- **English**, Full Professional Proficiency